What is claimed is:

1. A method comprising:

translating a design description into configurations for a plurality of processing elements on a single integrated circuit; and

setting at least one packet size for packet communications between the plurality of processing elements on the single integrated circuit.

2. The method of claim 1 wherein translating comprises partitioning the design into a plurality of functions.

3. The method of claim 2 wherein translating further comprises compiling the plurality of functions to code to run on at least one of the plurality of processing elements.

4. The method of claim 1 further comprising profiling a design represented by the configurations for the plurality of processing elements.

5. The method of claim 4 further comprising changing a power supply voltage value in response to the profiling.

6. The method of claim 4 further comprising changing a clock frequency in response to the profiling.

7. The method of claim 4 further comprising changing the at least one packet size in response to the profiling.

8. The method of claim 4 wherein profiling produces information describing latency.

9. The method of claim 4 wherein profiling produces information describing throughput.

10. The method of claim 4 further comprising comparing user constraints with output from the profiling.

11. The method of claim 10 wherein the user constraints include latency.

12. The method of claim 10 wherein the user constraints include throughput.

13. The method of claim 4 further comprising modifying parameters of the processing elements in response to the profiling.

14. A method comprising:

dividing a design description into a plurality of functions;

compiling at least one function into machine code to run on a first processing element;

translating at least one other function into a configuration for a second processing element; and

setting a packet size for packet communications between the first and second processing elements.

15. The method of claim 14 further comprising generating configuration packets to configure an integrated circuit that includes the first and second processing elements.

16. The method of claim 15 further comprising configuring the integrated circuit with the configuration packets.

17. The method of claim 14 wherein translating at least one other function comprises translating a plurality of other functions into a configuration for the second processing element.

18. The method of claim 14 further comprising profiling a design with the configuration packets.

19. The method of claim 18 further comprising modifying the packet size in response to the profiling.

20. The method of claim 18 further comprising modifying a power supply voltage of the first processing element in response to the profiling.

21. The method of claim 18 further comprising modifying a power supply voltage of the second processing element in response to the profiling.

22. The method of claim 18 further comprising modifying a clock frequency of the first processing element in response to the profiling.

23. The method of claim 18 further comprising modifying a clock frequency of the second processing element in response to the profiling.

24. An apparatus including a medium to hold machine-accessible instructions that when accessed result in a machine performing:

reading a design description;

compiling the design description to configure a plurality of processing elements; and

determining a packet size for communications between at least two of the plurality of processing elements.

25. The apparatus of claim 24 wherein the machine-accessible instructions when accessed further result in the machine performing:

profiling the design; and

modifying at least one parameter in response to the profiling.

26. The apparatus of claim 25 wherein modifying at least one parameter comprises modifying a clock rate of at least one of the plurality of processing elements.

27. The apparatus of claim 25 wherein modifying at least one parameter comprises modifying the packet size.

28. An electronic system comprising:

a processing element; and

a static random access memory to hold instructions that when accessed result in the processing element performing reading a design description, compiling the design description to configure a plurality of processing elements, and determining a packet size for communications between at least two of the plurality of processing elements.

29. The electronic system of claim 28 wherein the instructions when accessed further result in the processing element performing profiling the design, and modifying at least one parameter in response to the profiling.

30. The electronic system of claim 29 wherein modifying at least one parameter comprises modifying the packet size.